Attorney Docket No. YOR920030375US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Jose A. Tierno
Docket No.: YOR920030375US1
Serial No.: 10/668,562
Filing Date: September 23, 2003
Group: 2611
Examiner: Leila Malek

Title: Methods and Apparatus For Snapshot-Based Equalization of a Communications Channel

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APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants (hereinafter referred to as "Appellants") hereby appeal the final rejection, dated October 31, 2008, of claims 1-23 of the above-identified application.

REAL PARTY IN INTEREST

The present application is assigned to International Business Machines Corporation. The assignee, International Business Machines Corporation, is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

The present application was filed with claims 1-23, all of which remain pending. Claims 1, 11 and 21 are the pending independent claims.

Claims 1-23 stand finally rejected under 35 U.S.C. §103(a). Claims 1-23 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a method of equalizing an input signal received from a communications channel, comprising the steps of: generating at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal; and compensating for distortion associated with the communications channel based on at least a portion of the at least one generated sampling.

An illustrative embodiment includes a method of equalizing an input signal received from a communications channel (see the specification at, for example, page 6, lines 21-22, with reference to FIG. 4: "Equalization system 400 receives an input signal from the data communications channel (not shown).") As described in the specification at, for example, page 6, lines 9-13, with reference to FIG. 4, the method includes a step of generating (e.g., by snapshot module 404) at least one sampling from the received input signal based on a clock signal (e.g., low frequency sampling clock 502 in FIG. 5; see the specification at, for example, page 7, lines 10-27) unrelated to a clock signal used to recover data associated with the received input signal, and a step of compensating (e.g., by equalization algorithm 406) for distortion associated with the communications channel based on at least a portion of the at least one generated sampling.

Independent claim 11 recites an apparatus for equalizing an input signal received from a communications channel. The apparatus comprises a memory and at least one processor coupled to the memory. The at least one processor is operative to generate at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data

associated with the received input signal; and compensate for distortion associated with the communications channel based on at least a portion of the at least one generated sampling.

An illustrative embodiment includes an apparatus for equalizing an input signal received from a communications channel (see the specification at, for example, page 6, lines 21-22, with reference to FIG. 4: "Equalization system 400 receives an input signal from the data communications channel (not shown).") As described in the specification at, for example, page 9, lines 21-26, the apparatus comprises a memory and at least one processor coupled to the memory. As described in the specification at, for example, page 6, lines 9-13, with reference to FIG. 4, the processor is operative to generate (e.g., by snapshot module 404) at least one sampling from the received input signal based on a clock signal (e.g., low frequency sampling clock 502 in FIG. 5; see the specification at page 7, lines 10-27) unrelated to a clock signal used to recover data associated with the received input signal, and to compensate (e.g., by equalization algorithm 406) for distortion associated with the communications channel based on at least a portion of the at least one generated sampling.

Independent claim 21 recites an equalization system responsive to an input signal received from a communications channel. The system comprises a sampling module which generates at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal. The system further comprises a filter which compensates for distortion associated with the communications channel based on an equalization algorithm which is responsive to at least a portion of the at least one sampling generated by the sampling module.

An illustrative embodiment shown in FIG. 4 includes an equalization system (e.g., 400 in FIG. 4) responsive to an input signal received from a communications channel (see the specification at, for example, page 6, lines 21-22, with reference to FIG. 4: "Equalization system 400 receives an input signal from the data communications channel (not shown)."). As described in the specification at, for example, page 6, lines 9-13, the system comprises a sampling module (e.g., snapshot module 404 in FIG. 4), which generates at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal; and a

filter (e.g., programmable filter 402 in FIG. 4), which compensates for distortion associated with the communications channel based on an equalization algorithm (e.g., 406 in FIG. 4) which is responsive to at least a portion of the at least one sampling generated by the sampling module.

Illustrative embodiments of the claimed invention provide a number of advantages relative to conventional arrangements. For example, as described in the specification at page 9, lines 12-20, by using a sampling clock that is independent of (unrelated to) the clock and data recovery (CDR) circuit of the receiver, an illustrative embodiment of the claimed equalization technique can operate stand-alone, i.e., without needing input from the CDR circuit for operation.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 3, 9-11, 13 and 19-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,222,101 (hereinafter "Ariyavisitakul") in view of U.S. Patent No. 5,260,836 (hereinafter "Yada").

2. Claims 2 and 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ariyavisitakul in view of Yada further in view of U.S. Patent Application Publication No. 2004/0062326 (hereinafter "Hsu").

3. Claims 4 and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ariyavisitakul in view of Yada further in view of U.S. Patent Application Publication No. 2003/0086339 (hereinafter "Dally").

4. Claims 5, 6, 8, 15, 16 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ariyavisitakul in view of Yada further in view of U.S. Patent Publication No. 2004/0243258 (hereinafter "Shattil").

5. Claims 7 and 17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ariyavisitakul, Yada and Shattil, and further in view of U.S. Patent No. 6,570,944 (hereinafter "Best").

ARGUMENT

1. Rejection of claims 1, 3, 9-11, 13 and 19-23 under §103(a) over Ariyavisitakul and Yada.

Claims 1, 3, 9-11, 13 and 19-22

Appellants submit that the Examiner has failed to establish a proper case of obviousness in the §103(a) rejection of claims 1, 3, 9-11, 13 and 19-23 over Ariyavisitakul and Yada, in that the Ariyavisitakul and Yada references, even if assumed to be combinable, fail to teach or suggest all the claim limitations, and in that no cogent motivation has been identified for combining the references or modifying the reference teachings to reach the claimed invention.

Independent claim 1 is directed to a method of equalizing an input signal received from a communications channel, comprising the steps of: generating at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal; and compensating for distortion associated with the communications channel based on at least a portion of the at least one generated sampling.

In an illustrative embodiment of the present invention (FIG. 4), equalization system 400 receives an input signal from the data communications channel. The input signal is provided to programmable filter 402 whose filtering characteristics are set by filter parameters. The values for the filter parameters are provided by equalization algorithm 406. The filtering characteristics of filter 402 are adaptively set such that distortion associated with the communications channel is compensated for, i.e., canceled or, at least, substantially canceled. Snapshot module 404 samples the output of programmable filter 402, based on a clock (low-frequency sampling clock) that is unrelated to (e.g., independent of) the clock used to recover data, and provides a snapshot of the input signal to equalization algorithm 406 such that the algorithm can adapt the filter parameters, based on the snapshot, so as to compensate for distortion in the input signal caused by the channel. The adaptive loop of sampling the input signal (via snapshot module 404), adjusting the filter parameter values (via equalization algorithm 406) and applying the filtering parameter values (via programmable filter 402) to modify the input signal may continue until distortion in the input signal equals or falls below some maximum acceptable distortion threshold value.

Thus, as further explained at page 9, lines 12-20, of the present specification, by using a sampling clock that is independent of (unrelated to) the clock and data recovery (CDR) circuit of the receiver, the claimed equalization technique can operate stand-alone, i.e., without needing input from the CDR circuit for operation.

The Examiner, in formulating the §103(a) rejection of claim 1, argues that each and every one of the above-noted limitations of claim 1 is met by the collective teachings of Ariyavisitakul and Yada. Below, Appellants explain how such portions of Ariyavisitakul and Yada fail to teach or suggest what the Examiner contends that they teach or suggest. While Appellants may refer from time to time to each reference alone in describing its deficiencies, it is to be understood that such arguments are intended to point out the overall deficiency of the cited combination.

As conceded by the Examiner, Ariyavisitakul fails to disclose at least the limitation of the clock signal that is the basis of generating at least one sampling being unrelated to a clock signal used to recover data. More particularly, the Ariyavisitakul reference, at column 12, lines 14-15, teaches the symbol timing to be the same as the optimum sampling time for each symbol. Assuming for the sake of argument, that the symbol timing of Ariyavisitakul is the frequency at which the received input signal generates at least one sampling, and the optimum sampling time is a clock signal used to recover data associated with the received input signal, Ariyavisitakul fails to anticipate the limitation at issue since, in Ariyavisitakul, the symbol timing and the optimum sampling time are the same. In contrast, the limitation at issue discloses of generating at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal. Although column 12, lines 21-22 of Ariyavisitakul refers to transmitter and receiver clocks, whether Ariyavisitakul discloses a different transmitter clock from the receiver clock is irrelevant to the claim rejection. It is the receiver clock that is used to perform data recovery, not the transmitter clock. And as such, it is clear that Ariyavisitakul discloses that sampling is done using a clock related to the data recovery clock. Thus, Ariyavisitakul fails to anticipate the recited limitation.

The Examiner looks to the Yada reference to supplement the above-noted deficiencies of Ariyavisitakul as applied to claim 1. However, the Yada reference also fails to teach or suggest

"generating at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal," as recited in claim 1. The Examiner refers to FIGs. 1A and 1B of Yada which shows an ADC 4, an equalizer 5, a data detector 6 and a PLL circuit 7. The Examiner concludes that the sampling clock Fs is not related to the PLL clock used by the data detector. However, this interpretation is incorrect. As explained at column 8, lines 63-68, of Yada, "data detector 6 [is] supplied with a clock generated by phase locked loop (PLL) circuit 7, the latter being coupled to the output of the waveform equalizer to extract a clock from the waveform equalized digitized audio signal supplied thereto." Thus, the clock used by the data detector 6 is extracted from the equalizer output signal which was sampled at the rate of clock Fs (ADC clock), and therefore the two clocks are related.

In the final Office Action at page 2, the Examiner contends: "Yada does not indicate that the extracted clock is the clock used by ADC 4. Yada specifically states extracting a (and not the) clock signal from the waveform equalized digitized audio signal. Therefore the clock used by ADC 4 is not the clock used by data detector 6."

However, the claim does not merely call for the clocks to be non-identical. Rather, the claim calls for the clocks to be unrelated. It is without doubt that the clock used by data detector 6 in Yada is related to the clock used by ADC 4, since the clock used by data detector 6 is extracted from the signal that was sampled at clock Fs, i.e., the clock used by ADC 4. By way of further support for Appellants assertion that clock Fs is related to the clock used by data detector 6, the Examiner's attention is respectfully directed to column 7, lines 28-43, where it is clearly explained that clock Fs is generated to be in accord with the audio signal being reproduced ("to be compatible with the sampling frequency used for recording, the frequency Fs of the clock signal supplied to ADC 4 for sampling the multiplexed signals recovered from the playback heads may be represented as Fs = 8fs."). This is, in fact, why the clock used by data detector 6 in Yada can be extracted from the waveform equalized digitized audio signal (i.e., because the two clocks are related).

Thus, the Yada reference fails to supplement the above-noted deficiencies of Ariyavisitakul as applied to claim 1. Accordingly, it is believed that the teachings of Ariyavisitakul and Yada fail to meet the limitations of claim 1.

Moreover, even if the Examiner could somehow establish that all aspects of the invention recited in claim 1 were individually known in the art, such arguments are insufficient to establish a *prima facie* case of obviousness. See, e.g., *KSR International Co. v. Teleflex Inc.*, 127 SCt 1727, 1741, 82 USPQ2d 1385, 1396 (U.S. 2007) ("[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.") Specifically, the Examiner must provide an explicit "reason to combine the known elements in the fashion claimed by the patent at issue." *Id.*

Appellants respectfully submit that Yada is not analogous prior art and therefore cannot form the basis for a rejection under 35 U.S.C. §103. See, e.g., MPEP 2141.01(a); *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992) ("In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned."); *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992) ("A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem.").

Indeed, in *In re Clay*, the court disagreed with the PTO's argument that the reference and claimed inventions were part of the same endeavor, "maximizing withdrawal of petroleum stored in petroleum reserves," and instead found that a reference was not reasonably pertinent to the problem with which the inventor was concerned because a person having ordinary skill in the art would not reasonably have expected to solve the problem of dead volume in tanks for refined petroleum by considering a reference dealing with plugging underground formation anomalies. See also *Wang Laboratories, Inc. v. Toshiba Corp.*, 993 F.2d 858, 26 USPQ2d 1767 (Fed. Cir. 1993), in which the court expressly rejected an argument that a reference to a single in-line memory module (SIMM) for an industrial controller was in the same field of endeavor as a patent application directed to a SIMM for installation on a printed circuit motherboard for use in personal computers merely because both related to memories; rather, the reference was found to be in a different field of endeavor because it

involved memory circuits in which modules of varying sizes may be added or replaced, whereas the claimed invention involved compact modular memories.

There has been no showing in the present §103(a) rejection of claim 1 of objective evidence of record that would motivate one skilled in the art to combine the completely disparate teachings of Ariyavisitakul (directed to a radio communication system) and Yada (directed to an audio tape player system) to produce the particular limitations in question. Rather, the Examiner merely asserts that it "would have been obvious to one of ordinary skill in the art at the time of invention to use a clock for sampling the received signal unrelated to the clock used for data recovery purposes to make the process of data recovery faster (i.e., without spending time on recovering the clock of the transmitter and by using receiver's local clock)."

Appellants respectfully submit that this is a conclusory statement of the sort rejected by both the Federal Circuit and the U.S. Supreme Court. See *KSR*, 127 S.Ct. at 1741, 82 USPQ2d at 1396, quoting *In re Kahn*, 441 F. 3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.").

Furthermore, Appellants note that the Office Action claims that using a clock signal is inherent in Ariyavisitakul. However, Ariyavisitakul does not contain the disclosure which is necessary to support a rejection of a claim on the basis of inherency.

Specifically, in "relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) Moreover, the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. See, e.g., *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981).

The evidence provided by the Examiner "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by

persons of ordinary skill." *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). Appellants respectfully submit that the conclusory statements proffered by the Examiner fail to satisfy these requirements.

For at least these reasons, Appellants assert that claim 1 is patentable over Ariyavisitakul and Yada. Independent claims 11 and 21 include limitations similar to those of claim 1, and are therefore believed allowable for reasons similar to those described above with reference to claim 1.

Dependent claims 3, 9, 10, 13, 19, 20 and 22 are allowable at least by virtue of their dependency from claims 1, 11 and 21. Accordingly, withdrawal of the §103(a) rejection of claims 1, 3, 9-11, 13 and 19-22 is respectfully requested.

Claim 23

Claim 23 is allowable at least by virtue of its dependency from independent claim 21. Furthermore, this claim defines separately patentable subject matter. Specifically, claim 23 includes a limitation wherein the equalization system is independent of a clock and data recovery system of the data receiver. In an illustrative embodiment described in the specification at, for example, page 9, lines 12-20, an equalizer can operate stand-alone without needing input from the CDR circuit for operation.

In the Office Action at page 7, last paragraph, the Examiner argues that FIG. 1 of "Yada discloses that the equalization system 5 is independent of a clock and data recovery system 6 of the data receiver." However, Appellants respectfully submit that FIG. 1 of Yada clearly shows an arrangement in which waveform equalizer 5 is coupled to data detector 6. Thus, the relied-upon portion of Yada not only fails to supplement Ariyavisitakul so as to meet the limitations of dependent claim 23, but in fact teaches directly away therefrom.

2. Rejection of claims 2 and 12 under §103(a) over Ariyavisitakul, Yada and Hsu.

Appellants respectfully assert that Hsu fails to remedy the above-noted failure of Ariyavisitakul and Yada to teach or suggest the limitations of the independent claims. Thus, claims 2 and 12 are patentable at least by virtue of their dependency from claims 1 and 11.

3. Rejection of claims 4 and 14 under §103(a) over Ariyavisitakul, Yada and Dally.

Appellants respectfully assert that Dally fails to remedy the above-noted failure of Ariyavisitakul and Yada to teach or suggest the limitations of the independent claims. Thus, claims 4 and 14 are patentable at least by virtue of their dependency from claims 1 and 11.

Furthermore, these claims define separately patentable subject matter. Specifically, claims 4 and 14 include limitations wherein the sampling clock signal has a lower frequency than the data recovery clock signal. In an illustrative embodiment described in the specification at, for example, page 5, lines 6-10, and page 9, lines 17-19, a low-frequency sampling clock signal is used such that the snapshot circuit is operated with a very low duty cycle, thereby allowing the circuit to be kept on continuously without incurring a power penalty.

In the Office Action at page 8, last paragraph, the Examiner argues that paragraphs [0060] and [0061] of Dally suggest the aforementioned limitation of claim 4 wherein the sampling clock signal has a lower frequency than the data recovery clock signal. Appellants respectfully submit that the relied-upon portion of Dally in fact teaches away from the limitation at issue by suggesting that an undesirable "phase lag" occurs when the sample clock is slower than the data clock.

As recently noted by the Supreme Court, "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious." *KSR*, 82 USPQ2d at 1395 (citing *United States* v. *Adams*, 383 U.S. 39, 51-52, 148 USPQ 479, 484 (1966)).

4. Rejection of claims 5, 6, 8, 15, 16 and 18 under §103(a) over Ariyavisitakul, Yada and Shattil.

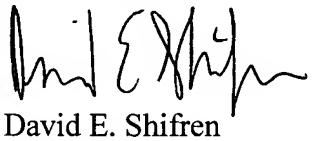
Appellants respectfully assert that Shattil fails to remedy the above-noted failure of Ariyavisitakul and Yada to teach or suggest the limitations of the independent claims. Thus, claims 5, 6, 8, 15, 16 and 18 are patentable at least by virtue of their dependency from claims 1 and 11.

5. Rejection of claims 7 and 17 under §103(a) over Ariyavisitakul, Yada, Shattil and Best.

Appellants respectfully assert that Best fails to remedy the above-noted failure of Ariyavisitakul, Yada and Shattil to teach or suggest the limitations of the independent claims. Thus, claims 7 and 17 are patentable at least by virtue of their dependency from claims 1 and 11.

In view of the above, Appellants believe that claims 1-23 are in condition for allowance, and respectfully request reversal of the pending rejections.

Respectfully submitted,



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CLAIMS APPENDIX

1. A method of equalizing an input signal received from a communications channel, comprising the steps of:

generating at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal; and

compensating for distortion associated with the communications channel based on at least a portion of the at least one generated sampling.

2. The method of claim 1, wherein the sampling generation step further comprises the steps of:

generating multiple phases of the sampling clock signal; and

sampling the received input signal at the respective multiple phases of the sampling clock signal to generate respective multiple samples.

3. The method of claim 1, wherein the distortion compensating step further comprises the steps of:

setting one or more parameter values based on the at least a portion of the at least one generated sampling; and

applying the one or more parameter values to the received input signal.

4. The method of claim 1, wherein the sampling clock signal has a lower frequency than the data recovery clock signal.

5. The method of claim 1, wherein the sampling generation step further comprises the step of validating the at least one generated sampling.

6. The method of claim 5, wherein the validating step further comprises comparing samples of the at least one generated sampling to a validation threshold.

7. The method of claim 5, wherein the validating step further comprises the steps of:

generating leading edge samples and trailing edge samples from the received input signal; and

varying an eye center threshold to determine the validity of the at least one generated sampling.

8. The method of claim 5, wherein the validating step further comprises discarding samples of the at least one generated sampling that are determined to be invalid.

9. The method of claim 1, wherein the communications channel is a digital communications channel.

10. The method of claim 1, wherein the equalization is performed in accordance with a data receiver coupled to the communications channel.

11. Apparatus for equalizing an input signal received from a communications channel, comprising:

a memory; and

at least one processor coupled to the memory and operative to: (i) generate at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal; and (ii) compensate for distortion associated with the communications channel based on at least a portion of the at least one generated sampling.

12. The apparatus of claim 11, wherein the sampling generation operation further comprises generating multiple phases of the sampling clock signal, and sampling the received input signal at the respective multiple phases of the sampling clock signal to generate respective multiple samples.

13. The apparatus of claim 11, wherein the distortion compensating operation further comprises setting one or more parameter values based on the at least a portion of the at least one generated sampling, and applying the one or more parameter values to the received input signal.

14. The apparatus of claim 11, wherein the sampling clock signal has a lower frequency than the data recovery clock signal.

15. The apparatus of claim 11, wherein the sampling generation operation further comprises validating the at least one generated sampling.

16. (Currently Amended) The apparatus of claim 15, wherein the validating operation further comprises comparing samples of the at least one generated sampling to a validation threshold.

17. The apparatus of claim 15, wherein the validating operation further comprises generating leading edge samples and trailing edge samples from the received input signal, and varying an eye center threshold to determine the validity of the at least one generated sampling.

18. The apparatus of claim 15, wherein the validating operation further comprises discarding samples of the at least one generated sampling that are determined to be invalid.

19. The apparatus of claim 11, wherein the communications channel is a digital communications channel.

20. The apparatus of claim 11, wherein the equalization apparatus is associated with a data receiver coupled to the communications channel.

21. An equalization system responsive to an input signal received from a communications channel, comprising:

a sampling module, the sampling module generating at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal; and

a filter, the filter compensating for distortion associated with the communications channel based on an equalization algorithm which is responsive to at least a portion of the at least one sampling generated by the sampling module.

22. The equalization system of claim 21, wherein the equalization system is part of a data receiver.

23. The equalization system of claim 22, wherein the equalization system is independent of a clock and data recovery system of the data receiver.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.